Fusion of DFT and Test Engg to optimize manufacturing cost

ndustry outlook towards Test Engineering

SOC Manufacturing and supply chain involve multiple phases from Architecture, design, verification, physical design & fabrication to testing and productization. In the current environment, test engineering (which is a critical component of product engineering) considerations are getting more stringent by the day as compared to the traditional design phase. This is glaring for a few industries, most notably automotive and medical sciences. For example, Pacemakers need very stringent testing procedures . A renowned automotive company based in the US, renowned in the driverless car space, has been part of accidents that have proven fatal. There are several other examples that can be attributed to defective design or manufacturing issues and many such faults can be identified during the post-manufacturing silicon tests that every chip goes through, if test architecture and implementation is up to the mark. Hence, the best approach is to have correct test architecture and get it implemented in the Pre-silicon phase for IPs, which will have multiplicative benefits across all designs. Correct test methodology will ensure that yield is not adversely impacted due to a faulty test program. Apart from stringent testing, one would also want to ensure good components are not rejected, thereby impacting the bottom line.

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Industry-specific safety standards and impact on Test Engineering

Governing bodies and standards are updated every year to ensure devices adhere to error tolerance levels. ISO26262 is the international standard for functional safety of electrical/electronic systems in the automotive industry defined by ISO in 2011. The standard also talks about ASIL (Automotive Safety Integrity Level) which classifies the inherent safety risk in any automotive ECU/system . Architects define the different DFT & test architectures based on different ASIL grades. Similarly, IEC 60601 is an umbrella of technical standards for the safety and performance of medical electrical equipment, published by the International Electro-technical Commission .

The tolerance for error in devices from these industries is nearly zero and is being defined not in Defective parts per Million (DPPM) but in Defective Parts per Billion (DPPB) today. That means, now, we cannot accept even a handful of defective parts in a one million sample, which represents a paradigm shift in the testing world. Higher test quality requirements imply the need for higher test coverage, and consequently, higher pattern count. In addition, beyond 97% test coverage, the test coverage to pattern count graph flattens out and demands more patterns to cover the remaining faults. For instance, for a typical digital chip, the pattern count may grow from 7K patterns to 50K if we add all these extra patterns on top of normal stuck at patterns.

The upward trending number of test patterns also implies that the pattern depth could exceed tester memory capacity. This would, in turn, mean that the tester needs to be loaded beyond one cycle to run all the patterns i.e. multi loading or change of tester itself to one supporting higher memory.

All this, basically, leads to ever-increasing test program cost consequently hitting the bottom line. The devices being tested go through wafer-level testing followed by packaged device testing to characterization at system level today. This leads to increased time to market as well which, in the current era of cutthroat competition, has repercussions on the market share.

VLSI industry changes adding to Test Engineering costs

FinFET, 3D chip stacking, lower technology nodes like 7nm are all trends in the technology industry with which, repeatedly, researchers have tried to make chips more compact and prudent. These trends have each posed newer challenges for test engineering. At lower technology nodes, the defects introduced by the fabrication process increase and so test engineering is expected to become more complex.

Test engineers address the challenges posed by each of these trends. For instance, for lower technology nodes, the defects increase and the yield challenges worsen. Advanced fault models

like Cell-aware try to address the problems posed by lower technology nodes but in turn introduce the baggage of high pattern count.

Proposed solution

One way to achieve test program optimization is bringing together test engineering expertise and DFT depth. The idea presented herein is that right from the pre-silicon architecture phase, DFT design correctness will ensure that there is optimum controllability and observability in the design. This should be done at the IP, ASIC and the SoC level. The addition and verification of DFT feature at a source level, i.e. IP level, is advocated in this article, so that this will never be neglected at the SOC level. We propose to have each IP fully testable in itself. Cross-domain expertise including VLSI domain and areas like AI/ML, data analytics, cloud infrastructure services, etc. give us a position to come up with a solution which has elements of analytics working as an enabling tool led by Test engineering expertise to define rules that lead to overall test cost reduction. Our approach results in bucketization, re-sequencing of patterns and moving of patterns up the test cycle (packaged device to wafer level) across various process corners. To cover process corners, the recommendation is creating optimization rule on devices across various lots, hence wafers. Please refer to the figure below for details on the methodology suggested in this article.

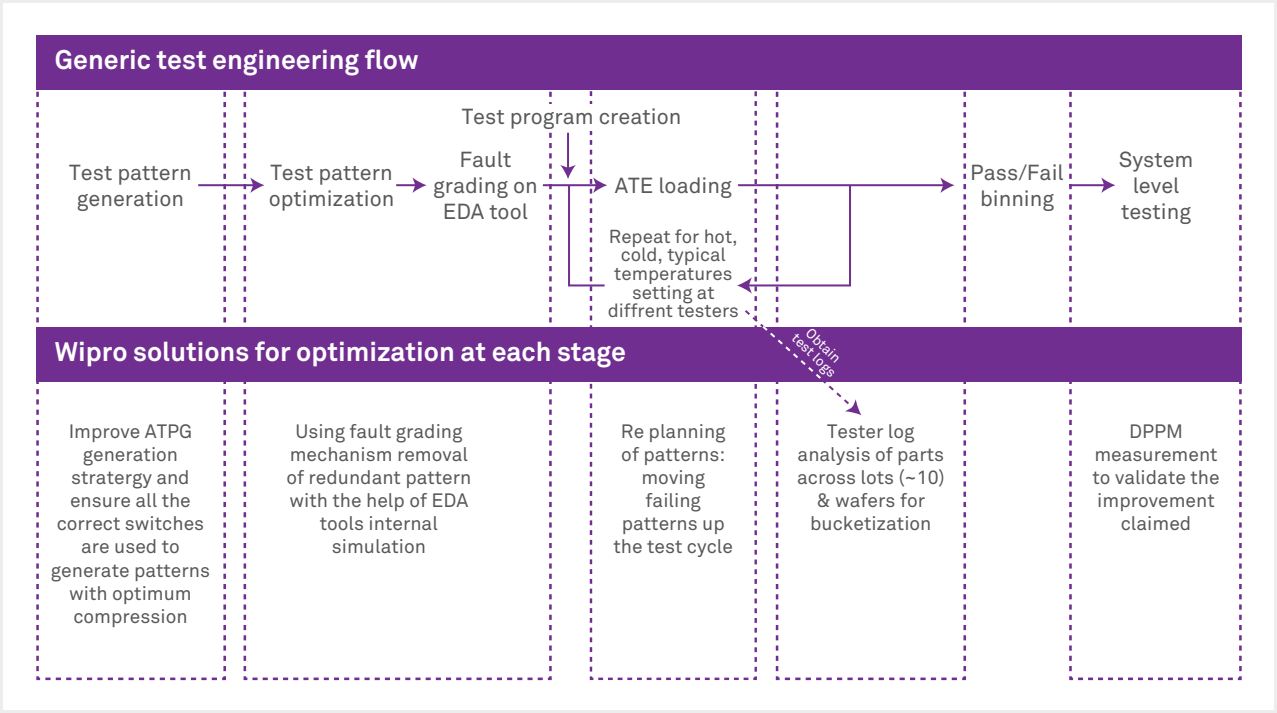

Figure 1: The building blocks of the insights tool

Conclusion

At the onset, the claimed outcome was reduction in pattern count. Twenty percent reduction in pattern count was achieved by using the methodology depicted in the above figure, thereby resulting in bottom line improvement. This proves that if DFT /ATPG and test engineering work as a single team with a common objective, better results are inevitable. This work has clearly proved our philosophy that if we move the problem of test engineering up in the supply chain by adding correct features in design and have better implementation, then test engineering will be a piece of cake.

The grit to go beyond traditional test engineering and work as consultants with our client has led to us getting very close to becoming the partner of choice for a major VLSI company for a lower technology node. Our SMEs are constantly redefining their test methodologies by working with foundry to add correct test logics needed for this latest tech node.

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Mohit has more than 25 years of experience with Significant time in DFT/Test/ Characterization and Low power IPs/SOC /Clock strategist and has worked in senior roles at Qualcomm, AMD, Ikanos, PLX (AVAGO), Teranetics, & Genesis Microchip prior to joining Wipro. He is a Postgraduate engineer with a Master's in Electrical Engineering and PG diploma in Interconnection technology from IISC Bangalore. He leads the DFT and TPE practice at Wipro. He has also received awards for his research paper on Test automation at NTU Singapore.

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